SRC/GRC Call for Proposals for 2022

Semiconductor Research Corporation (SRC)

- A non-profit organization with ~40 years of history and experiences
- Organize research needs from industry, academia, SIA, US Gov (DARPA, ERI, …), etc. for 5-30 years out
- Set up long-term goals: Decadal Plan, JUMP, …
- Solicit funding
  - $100+M/year and expanding
- Actively manage projects and funding, organize conferences and webinars, etc. on behalf of the sponsors

- MediaTek is a member of SRC
- MediaTek encourages professors to submit and participate SRC programs as part of the MediaTek MARC

Why SRC

- For university
  - Increase profs'/students' international visibility and collaboration opportunities
  - Generally higher funding level per project
  - Gain additional funding pipelines internationally
  - Gain ideas/inputs from industry and other universities internationally
  - Gain inputs from member companies about your proposals
  - Opportunities to access some of the US National Labs
- MediaTek has substantial project selection power for the money we put in → help for some proposals to get selected

SRC Programs at a Glance

1. Solicit ~$3.4B from US gov
2. May not be all managed by SRC
3. Funding may go to GRC and the new program to start in 2023

1st research roadmap across industry

1984
SRC 10y goals

1992
SIA/SRC NTRS

1998
ITRS

2017

2019

(SIA Blueprint)

2020 Decadal Plan

3x increase of federal investments in semiconductors

2023 →

1987
SEMATECH

1999
SRC-MARCO

2005
SRC-NRI

2017
SRC-JUMP/nCORE

Massive DARPA investments in semiconductors

Massive NSF and NIST investments in semiconductors

1. New program after JUMP?
2. Independent from GRC?

GRC is one independent path w/ multiple programs

Project Setup

- Normal proposal submission
  - GRC (annual cycle)
    - Program solicitations: two of every three years
    - Project start: typically in January
    - Program completion: when members agree
- Mini proposal solicitation
  - Special case only

Time: one quarter for each block activity

Q1

Begin annual cycle
- SRC collects and pools dues from all ~4- 8 members within each program.
- Industry members each appoint an employee to Technical Advisory Board (TAB) to govern program, chaired by SRC.

Q2

Select topics, solicit proposals
- TAB votes to select research topics relevant to their needs
- SRC writes and publishes solicitations for 3-year research projects. Each project ~$100K/yr., each program budget is ~$1.5- 2.5M/yr.

Q3

Proposal selection
- Collects proposals from academia
- Distributes proposals to TAB for voting, SRC tallies votes, determines selections
- Number of selected proposals depends on pooled dues, typically ~12 selected annually

Q4

SRC contracts researchers
- SRC contracts universities with research tasks, base contracts with T's & C's already in place
- Having contracted 250 universities 12,000 times with $2.2B total, SRC has well established process with favorable terms.

Program Timetable for 2022

	HWS	AIHW	AMS-CSD	PKG	LMD
WP Announcement	4/1	5/5	6/1	6/1	5/12
WP Submission Closed	4/28	6/2	6/22	6/22	6/9
Invite Proposals	5/31	7/7	7/25	7/25	7/13
Proposal Submission Closed	6/30	8/3	8/24	8/24	8/9
Program Start	10/1	1/1/2023	1/1/2023	1/1/2023	1/1/2023
Research Needs	PDF HWS	PDF AIHW	PDF AMS-CSD	PDF PKG	PDF LMD

- Schedule for 2022, can be updated as needed
- Decadal Plan for Semiconductors
  - https://www.src.org/about/decadal-plan/

Artificial Intelligence Hardware Program Overview

AIHW

https://www.src.org/program/grc/aihw/

Program Objective:

- Pushing the frontiers of artificial intelligence hardware across a broad spectrum of applications from the edge to the cloud

Members:

- AMD, Arm, IBM, Intel, NXP, Mubadala/GF, Qualcomm, Siemens EDA, Texas Instruments

Research topics

- Architectures for Power Efficient AI Acceleration
- Modeling, Analysis, and Simulation/Emulation of AI Hardware for Early System Exploration
- HW/SW Co-design of AI Compute Systems
- Secure and Robust A Hardware
- Interplay of AI and System Architecture/Microarchitect ure Design

AIHW: New Emphasis for 2022 Call

Higher Emphasis on Metrics: considerations include
• Peak, sustained, average; Performance, power, mapping efficiency; Training, inference; ISO-accuracy
• Inference accuracy (%)
• Inference robustness to antagonistic inputs (sensitivity)
• Inference/unit of energy (#/J)
• Throughput: inferences per unit time, training per unit time
• HW cost metric: MACs (or equivalent) required per unit time
• Memory metrics: local/global memory requirements (access time, latency, bandwidth, average per unit time and total energy per inference)
• Statistical performance guarantees
• Robustness and Explainability metrics
• Scalability across edge to cloud platforms
• Adaptability to different applications: Custom v/s generic AI acceleration

SRC Select Disclosure

AIHW Needs and the Seismic Shifts

1. Architectures for Power Efficient AI Acceleration
2. Modeling, Analysis, and Simulation/Emulation of AI Hardware for Early System Exploration
3. HW/SW Co-design of AI Compute Systems
4. Secure and Robust AI Hardware
5. Interplay of AI and System Architecture/Microarchitecture Design

Smart Sensing – The Analog Data Deluge	Memory & Storage – The Growth of Memory and Storage Demands	Communication – Communication Capacity vs. Data Generation	Security – ICT Security Challenges	Energy Efficient – Compute Energy vs. Global Energy Production
1, 2, 3, 4, 5	1, 2, 3, 4, 5	1, 2, 3, 4, 5	1, 2, 3, 4, 5	1, 2, 3, 4, 5

In each of the Seismic Shifts, there is a desire to use AI and ML to push the SoA and give new system functionality in a power-efficient manner. AIHW will be key to making this happen.

SRC Select Disclosure

AIHW Research Topical Areas

1	**Architectures for Power Efficient AI Acceleration**
1.1	New AI architectures, including but not limited to those using emerging devices and circuits, e.g., reduced precision/dynamic range computation, in-memory and near-memory computing based on charge-based and resistance-based memory devices, other NVM devices, mixed signal techniques, compute-in-DRAM, compute-in-cache, etc.
1.2	System-level integration solutions for emerging architectures, e.g., SoC, 3D, packaging, inter-chip / module communication, partitioning, etc.
1.3	Neuromorphic computing: algorithms and hardware for biologically plausible neuron models and learning rules, such as spiking neural networks, spike timing dependent plasticity, and bio-plausible deep learning
1.4	Probabilistic and approximate computing: use for AI/Machine Learning architectures as well as acceleration of probabilistic AI
1.5	High/Hyper-dimensional computing: algorithms, practical applications, energy efficient architectures
1.6	AI architectures using quantum computing
1.7	Resource efficient training and inference at the edge: self-teaching/adaptation/optimization/incremental-training of initial algorithms to local application conditions/needs within the strict computational/memory/power/costs constraints imposed by edge hardware/software including incremental learning systems (for example TinyML-type applications and reduced precision systems
1.8	End-to-end optimization schemes that span system-algorithm-architecture-circuit-technology stacks for minimizing energy per decision without compromising accuracy, throughput, and cost (power, area, performance), security/privacy constraints for AI systems consisting of sensors, pre- and post-processors, communication networks, and AI computer hardware
2	**Modeling, Analysis, and Simulation/Emulation of AI Hardware for Early System Exploration**
2.1	AI workload analysis and characterization
2.2	Efficient techniques for end-to-end performance/power/reliability modelling (cycle-accurate and analytical), simulation, emulation, and prototyping for exploration of AI systems
2.3	Benchmarks for emerging AI applications, and metrics for comparing AI systems (including applications in 2.4)
2.4	Application-level understanding and profiling of new AI applications including: a) recent deep learning networks (e.g. graph convolutional networks, energy-based models, foundation models) b) techniques for machine reasoning c) neuro-symbolic approaches d) Emerging application domains: examples include mmWave sensing, Industry 4.0, etc
2.5	Modeling infrastructure and techniques for AI computation at the edge/end node, including sensors, applications in 2.4, and more
2.6	Analysis and comparison of theoretical limits of algorithms and compute efficiency of AI systems (e.g. understanding theoretical limits of precision, sparsity, and compression)

AIHW Research Topical Areas

3	HW/SW Co-design of AI Compute Systems
3.1	Compilers and run-time management that map AI models/algorithms/computations to homogeneous or heterogeneous compute platforms including CPU/GPU/hardware accelerators
3.2	Compilers and run-time management that optimize data storage in compute in/near memory for reduced data movement
3.3	Run-time management of large number of accelerators/cores including virtualization and security of AI computation
3.4	Co-design of AI exploration, smart sensing, and training at the edge/end node
3.5	Systems supporting efficient self-supervised learning algorithms
3.6	Co-design of AI and HPC and other scientific applications, e.g. AI-based surrogate models
3.7	Co-design of CPU-friendly AI model training and inference algorithms including using AI-specific ISA extensions
3.8	Co-design of AI accelerators and interconnect/communication for power-performance-memory trade-offs
4	**Secure and Robust AI Hardware**
4.1	Methods and architectures that return a result and a rationale for that result, or that add explainability to existing AI/ML-based solutions
4.2	Architectures and algorithms to add fairness into machine learning algorithms and architectures while maintaining best possible performance and accuracy, even when trained with biased data
4.3	Architectures robust against both natural variations of input data and adversarial attacks to ensure stability of machine learning and AI decisions. Also, included under this are architectures capable of uncovering corruption/bias of training phase data and model integrity
4.4	Enhancing robustness by building prior knowledge about the task to be learned and/or about the training data into the ML solution, e.g. training with a potentially limited set of input data supplemented by rules-based data, and/or pre-wiring the neural network, and/or data synthesis to enlarge training data sets
4.5	Architectures with the ability to assess the functionality of its AI/ML process, so that a system with functional safety requirements can identify a malfunction and establish appropriate safety actions
4.6	Privacy and confidentiality preserving AI architectures and systems. Included in this are methods for anonymizing and securing training data. (e.g. Homomorphic Deep Learning)
5	**Interplay of AI and System Architecture/Microarchitecture Design**
5.1	AI-based or AI-inspired components that can be used in hardware designs: e.g., hardware predictors, prefetchers, resource management controllers, etc.
5.2	AI methods for optimization of hardware designs at the system, architecture and micro-architecture levels, e.g. communication, multi-media & graphics excluding CAD software optimizations (which are part of the CADT thrust)
5.3	AI-based design and optimization of AI accelerators and their integration in bigger systems
5.4	Synergistic advances in system design and AI/ML to improve performance, energy-efficiency, reliability/robustness, and security
5.5	AI-assisted operating system, run-time system, and hardware for thread scheduling, DVFS, power state transitions and other hardware resource management

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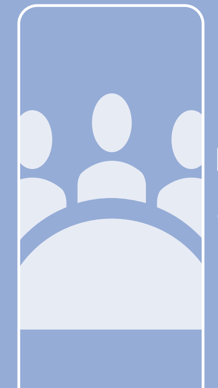
Analog Mixed-Signal (AMS-CSD)Program Overview

AMS-CSD

https://www.src.org/program/grc/ams-csd/

Program Objective:

- Extending the frontiers of analog/mixed-signal/RF design and technology by creating fundamental innovations in integrated circuits and systems that improve energy efficiency, health care, public safety, and security.



Members:

- AMD, Arm, IBM, Intel, MediaTek, NXP, Siemens EDA, Texas Instruments

Research topics

- Power Delivery and Management
- Wireline Communications
- Mm-wave and THz Circuits and Systems
- Wireless Communications
- Data Conversion
- Sensors and Information Extraction for Ubiquitous Data Collection
- AMS Devices and Models
- Clocking
- Efficient Circuits
- Reliable and Functionally Safe Circuit Design
- Analog Design Productivity and Automation

AMS-CSD Needs and the Seismic Shifts

https://www.src.org/program/grc/ams-csd/research-needs/2020/2020_src_ams-csd_needs.pdf

- A1. Power Delivery and Management
- A2. Wireline Communications
- A3. Mm-wave and THz Circuits and Systems
- A4. Wireless Communications
- A5. Data Conversion
- A6. Sensors and Information Extraction for Ubiquitous Data Collection
- A7. AMS Devices and Models
- A8. Clocking
- A9. Efficient Circuits
- A10. Reliable and Functionally Safe Circuit Design
- A11. Analog Design Productivity and Automation

Smart Sensing – The Analog Data Deluge

A1, A2, A3, A4, A5, A6, A7, A8, A9, A10, A11

Memory & Storage – The Growth of Memory and Storage Demands

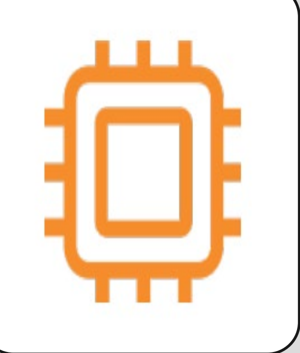
A1, A2, A3, A4, **A5**, A6, A7, **A8, A9, A10**, A11

Communication – Communication Capacity vs. Data Generation

A1, A2, A3, A4, A5, A6, A7, A8, A9, A10, A11

Security – ICT Security Challenges

A1, A2, A3, A4, A5, A6, A7, **A8, A9, A10**, A11



Energy Efficient – Compute Energy vs. Global Energy Production

A1, A2, A3, A4, A5, A6, A7, **A8, A9**, A10, A11

AMS-CSD Key Topics and Interests

- Alignment with Decadal Plan during 2022 solicitation
  - Smart sensing to address analog deluge:
    - Emphasis on AMS-CSD research need C6. sensors and Information Extraction for Ubiquitous Data Collection Transmission
  - Analog in Machine Learning at the Edge:
    - Analog in-memory Computing
    - Analog Mixed-Signal accelerator
    - Large Scale Field-Programmable analog array
    - Neuromorphic ADCs
    - Stochastic Analog Computing Circuits
  - Analog Design Productivity and Predictability
    - AMS Simulation/model benchmark
    - Re-use sim-automation tools
    - DFT
    - ML-based approaches to optimize design, layout, yield.
    - Methodologies and models to improve analog and mixed-signal simulation
  - AMS circuit design for heterogenous integration

Packaging Research Program Overview

https://www.src.org/program/grc/pkg/

Program Objective:

- Create and explore advanced evolutionary and revolutionary packaging technologies for reliably encapsulating and efficiently integrating microsystems

Members:

- Arm, IBM, Intel, MediaTek, NXP, Samsung, Texas Instruments

Research topics

- Design Enablement and Tools
- Interconnects including photonics
- Power Delivery and Thermal Management
- Metrology and Modeling
- Materials
- Heterogeneous Integration (HI)

Packaging Research Topical Areas

https://www.src.org//program/grc/pkg/research-needs/2021/2021_pkg_needs_document_final.pdf

Research Area	Key Topics
Design Enablement and Tools	• Modeling and characterization tools for new and existing architectures and structures that enable codesign of 2.5-D and 3-D architectures from (sub-) system level for energy efficiency, security, non-conventional computing/sensing, etc. • EM full-wave solvers for inhomogeneous, anisotropic lossy dielectrics and conductors, with algorithms optimized for both computation time and memory and approaching linear computational complexity • Novel design, modeling and simulation incorporating machine learning to speed up and cover more complexity, such as 3D floorplanning and optimization for SI/PI. • Board level test methodologies for packaging failures and predictive failure modeling to support rapid failure analysis and mitigation. Packaging co-design with emphasis on enabling cost-effective, high-precision/accuracy testing (to ppb levels)
Interconnects, including photonics	• High bandwidth electrical, optical and wired/waveguide (WG) interconnection mesh in 3D, such as a combination of electronic/optical circuits and a high number of wires/WGs at low loss, low cost, and high tolerance, applicable to inter- and intra-package connectivity involving multiple types of packages and sockets. Repairability/serviceability is also desired. • Architectures and structures to enhance isolation, etc. without degrading PPA.
Power Delivery and Thermal Management	• Future power delivery applications are expected to require transient current densities of 5 – 10 A/mm2 at 1 V or less • Driving to smaller form factors so the power delivery solutions should fit within the footprints of either the package or the die and have a small z-height. Hot-spot metrology and low-cost mitigation schemes including novel materials to address hot spots at thermal densities > 500 W/cm2 • Architectures and structures to mitigate security breach, such as SCA.
Metrology, Modeling, and Test	• Metrologies, test, and simulation that enable fundamental understanding of package performance and reliability, help improve manufacturability, and are critical for packaging technology development and optimization • High-resolution, non-destructive metrologies for failure analyses that are able to detect and resolve defects (such as voids, delamination, bump, die, corrosion, and interface delamination cracks) at a size scale of < 1 um
Materials including Solder and Wire-bonds	• Mechanical properties at least as good as tin-silver-copper (SAC) solder over a wide temperature window (-65°C to 150°C), i.e., modulus 20 – 60 GPa, CTE ~ 20 ppm/K, elongation > 35%, tensile strength > 55 MPa, shear strength > 30 MPa; creep, fatigue strengths, and fracture toughness (strain hardening exponents) at least equal to that of the SAC solders • Materials and structures to enable emerging device and applications, such as in-package optical WGs, low-temperature computing, etc.

SRC Select Disclosure

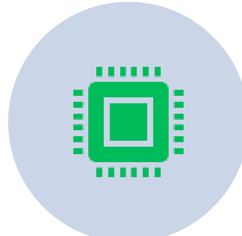
Alignment to Decadal Plan Seismic Shifts

https://www.src.org/about/decadal-plan/

PKG

At **THz frequencies and beyond (optical)**, interfaces to the outside world are challenged by parasitic effects from traditional resistance, capacitance and inductance to fringing, roughness, and index of refraction at multi-GHz frequencies

Integration of multiple technologies will be required and will not be possible on a single chip and/or require very closely coupled passives and smart sensors; advancements in 2.5D/3D integration will be required to handle mix of analog and digital technologies



Package-level integration utilizing heat sinks and air cooling is becoming limited by thermal constraints; while more exotic cooling solutions exist, these tend to be impractical in production environments due to the cost and support requirements

Memory is becoming a big part for all edge applications, where systems need to be more and more tailored to use cases and integrated through custom packages; flexibility for different use cases needs to be built into the design

Alignment to IEEE's Heterogenous Integration Roadmap

PKG

https://eps.ieee.org/technology/heterogeneous-integration-roadmap.html

- Heterogenous Integration Roadmap (HIR) can help shape our research needs
  - Focused on system-level integration and advanced packaging technologies that address expanding markets and enable continued progress (beyond Moore's Law and ITRS)

- Heterogeneous Integration is essential to maintain the pace of progress with higher performance, lower latency, smaller size, lighter weight, lower power requirement per function, and lower cost

Decadal Plan - HIR Convergence:

5 Seismic Shifts driving Technology Applications

HPC & Datacenter

Medical Wearables & Health

Autonomous Vehicles

Smart Mobile

Aerospace & Defense

IoT & IoE

Key Packaging Topics and Themes

Technical

- Heterogeneous Integration of microchips
- 2.5-D and 3-D architectures
- Interconnects, including photonics
- Power delivery and thermal management
- Metrology, modeling, and test
- Reliability
- Flexible packaging
- Solder joint, under bump metallization, and ball grid array
- Packaging for Autonomous and Electric vehicles
- Achievement of zero defects in automotive packaging
- Advanced Sensor Packaging
- Advanced wire bond packaging for low-cost packaging
- Battery Management
- Extreme environments like aeronautical, space, or cryogenics

Applications

- RF and mixed-signal
- High-performance computing
- Mobile
- Automotive
- Sensors
- IoT and IoE
- Wearable
- Medical
- Defense
- Power

Computer-Aided Design and Test Program Overview

CADT

https://www.src.org/program/grc/cadt/

Program Objective:

- Provides research leadership in electronic design automation by making available to members leading-edge university research results, techniques, and tools for the design and test of advanced electronic circuits and systems.

Members:

- Arm, IBM, Intel, NXP, Siemens EDA, Texas Instruments

Research topics

Functional Safety Tools And Techniques

- Safe Systems
- Data Mining and Failure Prediction
- Design for Functional Safety

System, Logic, and Physical Design Tools

- System Tools for Power Efficient High-Performance Designs, Long Term Reliability
- Tools for Design Robustness
- Analog Tools

Test

- Test of Machine Learning Systems
- Test Cost, Quality , and Yield Improvement
- High-Level Test, Validation, Diagnosis and Repair
- Analog, Mixed-Signal, RF, and High-Speed Test

Verification

- Verification of Machine-Learning Systems
- Machine Learning Techniques for Verification
- System-Level Verification
- Formal Technologies for Specification Design, and Verification

SRC Select Disclosure

New Topical Area for CADT

New Frontier for Scalable, Correctness-Assured Hardware Design

Moore's Inflection: "…the priorities we set today will determine whether the state of the electronics ecosystem becomes stagnant, rigid, and traditional, or grows to be dynamic, flexible, and innovative." –William Chappell, The Intertwined History of DARPA and Moore's Law, DARPA 2018

Challenge: New applications and workloads and driving rapid architecture innovations. However, 30-year old RTL design practice cannot keep up with the pace of innovation and the exponentially growing development complexity and cost, dominated by functional validation.

Vectors of Research Need:

- N1 Raise level of Abstraction in Hardware Design as A Continuation of Software Development
- N2 Design Implementation through Trusted Complier/Behavioral Synthesis Transformations
- N3 Provably-Correct Design Construction
- N4 Verification as an Integral Part of Design Evolution

CADT Needs and the Seismic Shifts

- Functionally Safe Tools and Techniques (FS)
- System, Logic, and Physical Design Tools (SLPD)
- Test (T)
- Verification (V)

Smart Sensing – The Analog Data Deluge	Memory & Storage – The Growth of Memory and Storage Demands	Communication – Communication Capacity vs. Data Generation	Security – ICT Security Challenges	Energy Efficient – Compute Energy vs. Global Energy Production
FS, SLPD, T, V	FS, SLPD, T, V	**FS, SLPD, T, V**	**FS, SLPD, T, V**	**FS, SLPD, T, V**

In each of the Seismic Shifts, there is a need to use EDA techniques to **model**, **simulate**, **verify**, and **test** the circuits and systems being built. As design moves to the system level, EDA techniques follow and incorporate more of the design. Also, with different applications (such as industrial or automotive) there are operational **safety** concerns which also need to be addressed especially in the field

CADT Research Topical Areas

https://www.src.org/program/grc/cadt/research-needs/2021/cadt_needs_2021.pdf

Functional Safety Tools and Techniques	
F1	Safe System
F2	Data Mining and Failure Prediction
F3	Design for Functional Safety
System, Logic, and Physical Design Tools (SLPD)	
S1	System Tools: Key Design Goals – Power Efficient High-Performance Designs, Long Term Reliability
S2	Tools for Design Robustness
S3	Analog Tools
Test	
T1	Test of Machine Learning Systems
T2	Test Cost, Quality, and Yield Improvement
T3	High-Level Test, Validation, Diagnosis and Repair
T4	Analog, Mixed-Signal, RF, and High-Speed Test
Verification	
V1	Verification of Machine-Learning Systems
V2	Machine Learning Techniques for Verification
V3	System-Level Verification
V4	Formal Technologies for Specification, Design, and Verification

Hardware Security Research Program Overview

https://www.src.org/program/grc/hws/

HWS

Program Objective:

- Developing strategies, techniques, and tools to provide assurance that electronic systems will perform as intended. Such assurance is a function of processes and tools integrated across design, architecture, manufacturing and distribution.

Members:

- AMD, Analog Devices, Arm, IBM, Intel, Mentor, Texas Instruments

Research topics

- Trusted Architectures and Hardware Security
- Security Techniques for Advance Technologies and Packaging
- Security Aspects of Embedded Software, Firmware, and Soft IP
- Security Assurance, Protection, and Verification
- Authentication, Attestation, and Provisioning

Hardware Security Stack Focus

Layered Defense-in-depth HW security strategy

Ecosystem security

Software and Application security

Firmware security

System-On-Chip security

Secure IP-to-IP Communication protocols

Register/Memory access controls

HW Root of Trust

- Our current mission:
  - To develop designs, analysis strategies, processes and tools for secure, trustworthy, reliable and privacy preserving chips, packaging, systems, **computing, and communications**.

Software Attacks to exploit Hardware vulnerability

Novel Attack Surfaces/Models

Side-Channel Attacks

Important Considerations

- Sophistication versus cost
  - Adding security features comes with a significant costs: in design time, in software code space, in hardware area, and in power consumption – need to drive down cost while driving up security
  - The absence of reliable metrics for security makes it even harder to evaluate the **"return on investment"** for different protection methods
  - It is a challenge to monetize security features, but the cost of security failures is easier to assess.
- System security versus component/feature security
  - Today's ecosystem relied on the System of Systems; it is necessary to enable secure connectivity and trusted data sharing enabling **"security by design"**
  - Security features protect a portion of the system, but multiple security features are not integrated well in a large System-On-Chip system leading to vulnerabilities
  - Many design processes are not security aware, create scoring/ranking system to evaluate various methods (design confidentiality and integrity) to avoid security vulnerabilities
- Research directions in support of these considerations
  - Flexible **"HW Root of Trust Primitives"** that enable solutions that remain secure during the life-cycle of the product
  - Viable **"security metrics"** to enable analysis, better threat mitigation and predictive capability against future attacks using AI/ML or other methods
  - **"Field upgradable security"** enhancements to recover from a breach and mitigate weaknesses.
  - Post Quantum Cryptography and Homomorphic Encryption
  - Improved monitoring to observe system behavior in the field to detect, predict, and recover from security attacks

Examples of new trends/areas of interest

- Trust as a service
- Security for near data processing architectures, novel data transfer technologies
- Automatic generation of threat models based on data
- Approximate computing in security and cryptography
- 6G Security for Communications
- Security Challenges caused by advanced packaging growth (2.5D/3D/HI)

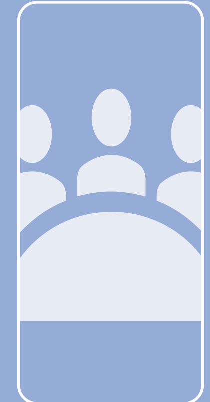
Logic and Memory Devices (LMD) Program Overview

LMD

https://www.src.org/program/grc/lmd

Program Objective:

- Explores advanced CMOS technology with emerging alternative concepts such as multiferroics, spintronics, photonics, and their 3D monolithic integration.



Members:

- AMD, Arm, IBM, Intel, Mentor(Siemens), Samsung, SK Hynix, TSMC, Veeco

Research topics

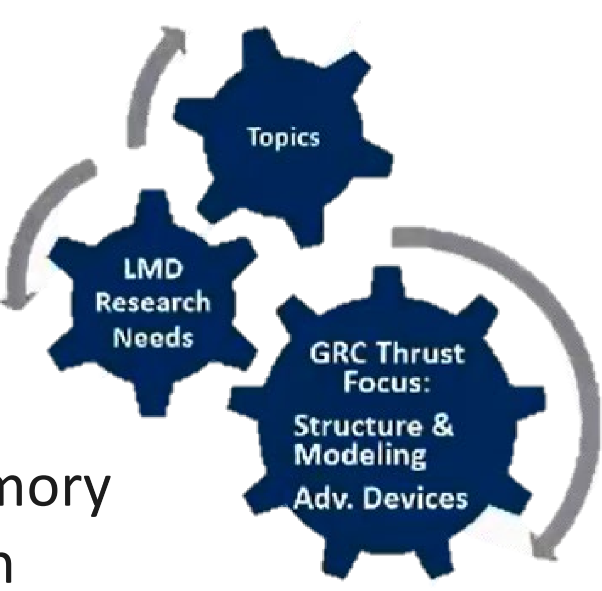
- Low-dimensional device Materials, Spintronics, disruptive high-performance energy-efficient BEOL compatible devices.
- Logic devices: MOSFETs with high-mobility channel materials, transistors based on tunneling, non-tunneling transports and phenomena, spin and magnetism, functional devices
- New concepts for contacts, junctions, and gate structures
- Memories: Scalable energy-efficient disruptive memory alternatives at various levels of the memory hierarchy form SRAM to DRAM, to NVM, analog memory devices
- Simulations, modeling, and fundamental understanding of devices, materials, and physical phenomena

LMD – Key Themes

8 Thrusts in the GRC programs: AIHW, AMS-CSD, CADT, ESH, HWS, LMD, NMP, PKG

Themes:

1) Logic devices:
   - Low dimensional transistors – AIHW, AMS-CSD, HWS
   - New concept for contacts, junctions, and gate structures – NMP
   - Monolithic Heterogenous 3D Integration (MH3D) – PKG
2) Memory devices:
   - NVM - NMP
   - Analog memory/ novel SRAM or DRAM – NMP
3) Selection device for memory arrays – Density booster of a memory
4) BEOL compatible devices – density & energy efficiency solution
5) Simulations – Future of semiconductor industry
6) Others



LMD Research Topical Areas

1) Logic devices:

1a) MOSFETs with high-mobility channel materials including low-dimensional 1D and 2D materials:

- 1D Materials (CNTs & Si-/III-V-based NWs, etc.)
- 2D Materials (Graphene, MoS_2, WSe_2, etc.)
- High-electron-mobility-transistors, HEMTs (GaN, SiC, etc.)

1b) Transistors based on spin and magnetism

1c) New concepts for contacts, junctions, and gate structures to said options in 2a and 2b)

1d) C(Complementary) FET and 3D integration, BEOL compatible devices

2) Memories:

2a) NVM: MRAM and SOT-MRAM, FeRAM, other novel concepts, PC/R-RAM, …

2b) Analog memories

2C Novel / Revolutionary SRAM and DRAM concepts that are denser / energy-efficient, scalable.

2d) Metrology for memory devices

3) Selection devices for cross-bar memory arrays

4) BEOL compatible Embedded devices

5) Simulations, modeling, and fundamental understanding of devices, materials, and physical phenomena

6) Other topics